REMARKS/ARGUMENTS

Reconsideration of the application is requested.

Claims 1-4 and 6-11 remain in the application. Claims 5 and 12 have been cancelled. Claims 10-11 have been previously withdrawn and rejoinder of claims 10-11 has been requested.

In item 1 on pages 2-4 of the above-mentioned Office action, claims 1-2, 4, 6, and 8 have been rejected as being unpatentable over Cho (US 6,087,718) in view of Lin et al. (US 6,593,649) under 35 U.S.C. § 103(a).

In item 2 on pages 5-8 of the above-mentioned Office action, claims 1-4 and 6-9 have been rejected as being unpatentable over Chang et al. (US 6,483,181) in view of Lin et al. under 35 U.S.C. § 103(a).

In item 3 on pages 8-9 of the above-mentioned Office action, claims 7 and 9 have been rejected as being unpatentable over Cho in view of Lin et al. and further in view of Chang et al. under 35 U.S.C. § 103(a).

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and

the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

> a first interposer layer or interposer film configured on said active surface of said first semiconductor chip, said first interposer layer or interposer film having first bonding fingers, first interposer lines and first bonding surfaces; and
>
> a second interposer layer or interposer film configured on said active surface of said second semiconductor chip, said second interposer layer or interposer film having second bonding fingers, second interposer lines and second bonding surfaces;
>
> each one of said plurality of first bonding connections connecting one of said first bonding surfaces on said first interposer layer or interposer film to said inner section of one of said plurality of flat conductors; and
>
> each one of said plurality of second bonding connections connecting one of said second bonding surfaces on said second interposer layer or interposer film to said transitional section of one of said plurality of flat conductors.

Cho fails to teach an interposer layer or interposer film configured on the active surface of the semiconductor chips. Also, it is not obvious from the teaching of Cho to provide an interposer layer or interposer film on the active surface of the semiconductor chips. Cho fails to provide any motivation for a person skilled in the art to modify the package and

fails to provide any reason for a person skilled in the art to provide an interposer layer or interposer film on the active surface of the semiconductor chips.

Even if a person skilled in the art were to be motivated to modify the package as taught by Cho, it is not obvious to look to the teaching of Lin et al.

The invention of the instant application addresses the problem of providing a more reliable connection between stacked semiconductor chips and the flat conductors of a leadframe. This problem could be addressed in a large number of ways, for instance by improving the bonding conditions. The provision of an interposer film is, therefore, not an obvious solution to the problem.

Even if a person skilled in the art were motivated to look in the prior art for methods by which the bond connections in a stacked leadframe-based semiconductor package could be improved, the structure of the invention of the instant application as claimed, namely the provision of the interposer layers on the active surfaces of the semiconductor chips, is not obvious from the teaching of Lin et al.

Lin et al. teach a method for providing an interposer layer structure so that the I/O pads can be relocated and a flexible rewiring structure can be provided on the surface of the chip. This enables semiconductor devices of different dimensions to be packaged in the same housing. Lin et al. provide no indication that the provision of an interposer layer on the active surface of stacked semiconductor chips in a leadframe-based package could lead to an improvement in the reliability of wire bonds between a semiconductor and a leadframe.

Similarly, Chang et al. fail to provide any motivation for a person skilled in the art to modify the stacked package of Chang et al. Even if a person skilled in the art were motivated to modify the package of Chang et al., it is not obvious from the teaching of Chang et al. or Lin et al., taken separately or considered together, to provide an interposer layer on the active surface of stacked semiconductor chips in a leadframe-based package.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claim 1. Claim 1 is, therefore, believed to be patentable over the art and since claims 2-4 and 6-9 are dependent on claim 1, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-4 and 6-9 are solicited. Rejoinder of method claims 10-11 is requested upon allowance of product claims under MPEP 821.04 ("if applicant elects claims directed to the product, and a product claim is subsequently found allowable, withdrawn process claims which depend from or otherwise include all the limitations of the allowable product claim will be rejoined").

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made. Please charge any fees which might be due with respect to 37 CFR Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

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